Towards the Formal Verification of a Distributed Real-Time Automotive System

NASA Formal Methods 2010

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Background

- Verisoft

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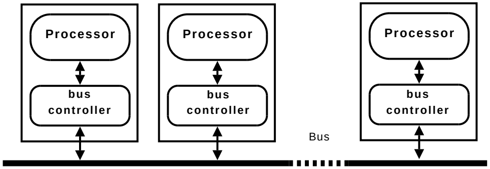
- implemented in ML
- Verilog (Shadrin), FPGAs (Endres)
- electronic control units (ECUs) interconnected by a bus

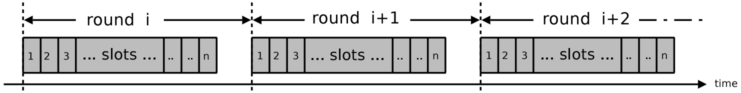


Automotive Real-Time System

Communication & Clock Synchronization

Each ECU has its local notion of time

- time is split into rounds
- each round consists of *n* slots



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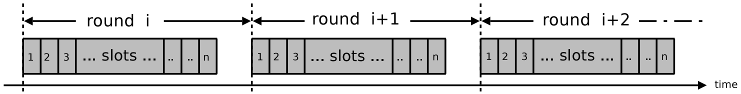

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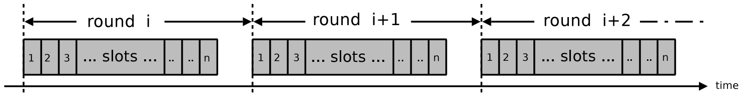

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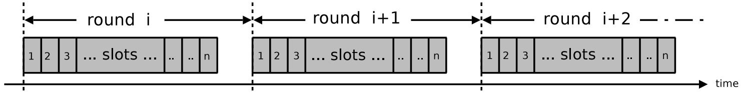

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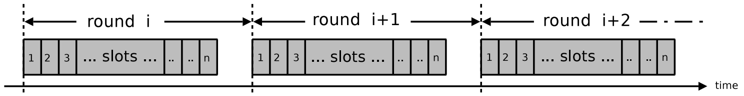

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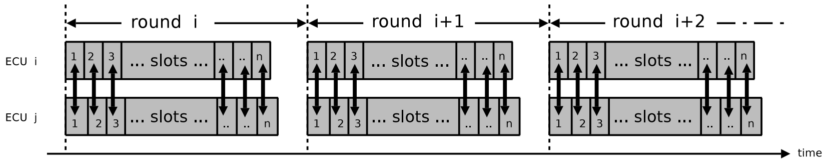

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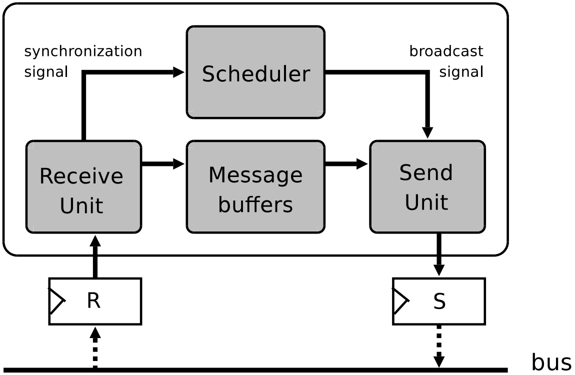
Bus Controller



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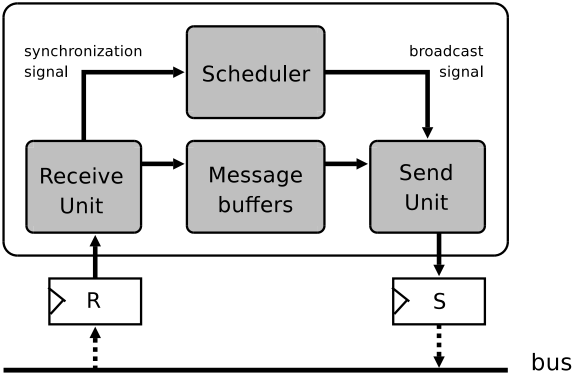

$$\forall \text{ real times } t : bus(t) = \bigwedge_{\forall \text{ ECU } i} analogSendRegisterValue_i(t)$$

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Top Level Theorem

Theorem (Overall Transmission Correctness)

At the end of each slot, the receive buffer of all ECUs is equal to the send buffer of the sending ECU at the beginning of that slot.

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3. message transmission: send buffer - bus - receive buffer (**1**,**2**)

□

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- Scheduler Correctness
    - proven by Boehm for three controllers (linked to master only)
    - after synchronization – no slot boundaries within transmission

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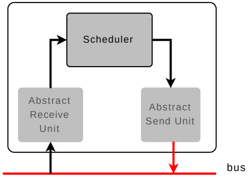

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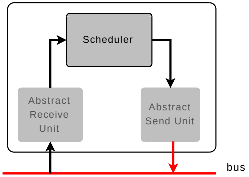

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- **a complete formalization and implementation of the entire model before proofs would by VERY helpful!**

Thank you!

Questions?